THE MU3E DATA ACQUISITION SYSTEM

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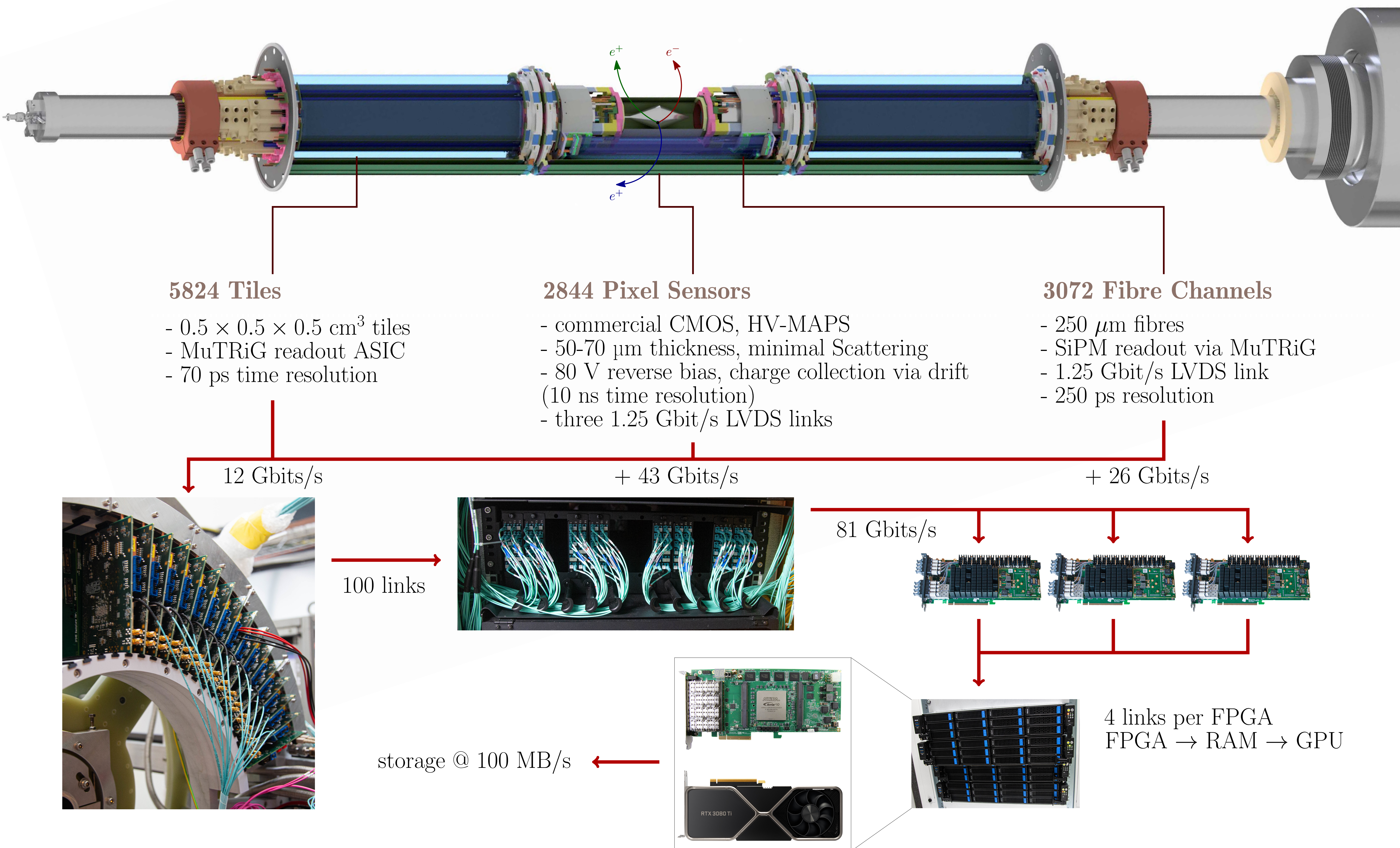## Summary

The *Mu3e* experiment is designed to search for the **C**harged **L**epton **F**lavor **V**iolating decay $\mu^+ \to e^+e^-e^+$. The aim is to reach a branching ratio sensitivity of 10^{-16}. The experiment is located at the Paul Scherrer Institute. The detector utilizes thin **H**igh-**V**oltage **M**onolithic **A**ctive **P**ixel **S**ensors for precise position measurement and scintillating fibre and tile detectors for precise time measurement. In a first phase the total data rate will reach **100 Gbit/s**. The stream of data is passed to **GPU filter farm** where full track and vertex reconstruction is performed to reduce data rate by factor of 100 for subsequent storage.

Mu3e Experiment

- Search for **CLFV** in the decay $\mu^+ \to e^+e^+e^-$
- Standard Model: BF $< 10^{-54} \to$ new physics
- SINDRUM (1988): BF $< \mathbf{10^{-12}}$
- Phase I: $\mathbf{10^{-15}}$ sensitivity at πE5 beamline (10^8 μ/s)
- Phase II: $\mathbf{10^{-16}}$ at upcoming **HiMB**: 10^9 μ/s
- Backgrounds: random combinations and internal conversion
  - need good momentum and time resolution

5824 Tiles

- $0.5 \times 0.5 \times 0.5$ cm^3 tiles
- MuTRiG readout ASIC
- 70 ps time resolution

2844 Pixel Sensors

- commercial CMOS, HV-MAPS
- 50-70 µm thickness, minimal Scattering
- 80 V reverse bias, charge collection via drift (10 ns time resolution)
- three 1.25 Gbit/s LVDS links

3072 Fibre Channels

- 250 µm fibres
- SiPM readout via MuTRiG
- 1.25 Gbit/s LVDS link
- 250 ps resolution

12 Gbits/s   + 43 Gbits/s   + 26 Gbits/s

100 links

81 Gbits/s

4 links per FPGA
FPGA → RAM → GPU

storage @ 100 MB/s

Inside magnet

- 112 front-end boards
- Configuration and control
- Data alignment and time sorting
- Operated in magnetic field and helium
- Intel Arria V FPGA
- 36 LVDS inputs per FEB at 1.25 Gbit/s from detector ASICs
- 10 ps jitter clock from Clock System

Switching Boards

- Align data, forward to filter farm
- Detector configuration
- 4×PCIe40 boards (developed for LHCb and ALICE)
- Intel Arria 10 FPGA
- 48 6.25 GBit/s optical links
- PCIe 3x8 interface to PC

Filter Farm

- Terasic DE5a-Net DDR4 boards
  - Data merging and data frame assembly
  - Forward data to GPU via DMA
  - Intel Arria 10 FPGA
  - 16 10 GBit/s optical links
  - PCIe 3x8 interface to PC

- NVIDIA GPU (3090 Ti and 4090):
  - Online track finding and fitting
  - 10^9 track fits each second on a single GPU
  - Vertex fit for $\mu \to 3e$ search
  - 10 GB/s input from detectors at 32 MHz frame rate
  - factor 100 rate reduction

Slow control and DAQ

- **M**aximum **I**ntegrated **D**ata **A**cquisition **S**ystem
- Web UI based DAQ control system
- 100 MB/s to disk (PSI Petabyte archive)

June 2025 data run: 16 us frame